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Application Brief

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Using the iFX780 FPGA in Hybrid 3.3V/5V Systems

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1.0 Introduction

The move from 5V to 3.3V supply voltages in the electronics industry is well under way. The requirements of low-power computers and shrinking process geometries have finally spurred semiconductor manufacturers to qualify many 5V component designs for 3.3V operation, as well as to design components for 3.3V operation from the start. While the laptop/notebook market, as well as other battery-operated markets, will make a complete change to 3.3V-only operation as quickly as component manufacturers will allow, other markets will not move nearly as fast. Many other electronic products will be hybrid 5V/3.3V products for some time.

Hybrid 5V/3.3V systems raise design issues that 5V-only or 3.3V-only systems do not. In addition to routing/switching of two power sources, designers must consider the effects components with different drive levels have on one another when they are connected together. This application brief summarizes the issues with respect to drive levels from 5V and 3.3V components in hybrid systems, and shows how the multi-voltage drive capability of Intel's iFX780 FLEXlogic FPGA device greatly simplifies the design of hybrid systems, while integrating a large number of PLDs or discrete logic devices into a single package.

A brief iFX780 product overview sets the context for the discussion.

2.0 Product Overview and I/O Summary

The iFX780 is the first member of Intel's FLEXlogic family of FPGA-class devices. The iFX780 is an 80 macrocell device that offers a fast, deterministic 10 ns t_{PD} from any input or I/O to any other I/O. It can operate in-system at speeds up to 80 MHz. Figure 1 shows a block diagram of the iFX780 device in the 132-pin package. The device is grouped into eight Configurable Function Blocks (CFBs); each CFB can be independently configured as a 24V10-type PLD or as a 128 deep x 10-bit wide bank of SRAM. This application brief does not discuss the advanced CFB and macrocell features of the device. For additional information on the architecture and features of the device, refer to the iFX780 FPGA data sheet (lit. order no: 290459) and other application briefs.

Of special note for hybrid systems is that fact that each CFB has its own output reference pin (VCCO) independent of the VCC pins. This allows the 10 output buffers for each CFB to swing from 0-3.3V or 0-5V by tying its respective VCCO pin to a 3.3V or 5V source. Outputs of a CFB can even start out in product life as 5V outputs to drive 5V devices and be shifted to 3.3V outputs when 3.3V devices are available via a manufacturing jumper on the VCCO pin. Dynamic shifting of output levels is also possible via a voltage switch on the VCCO pin. The core of the iFX780 (everything but the output buffers) requires 5V to operate. (Note that the 84-pin package has six VCCO pins rather than eight; two pairs of CFBs share a VCCO pin.)

Design tools allow outputs with like voltages to be assigned to the same CFBs, via a keyword in the source file, such as "5VOLT" or "3VOLT" (the exact keyword and syntax will vary depending on the tool used). Note that while keywords allow design tools to group signals together, the actual voltage level of CFB outputs is dependent on the VCCO pin.

An open-drain option for all outputs is available and is also supported by a source file keyword, such as "OPEN_DRAIN". The open-drain option is supported on an output-by-output basis and is configured during programming, but can be changed via in-circuit reconfiguration.

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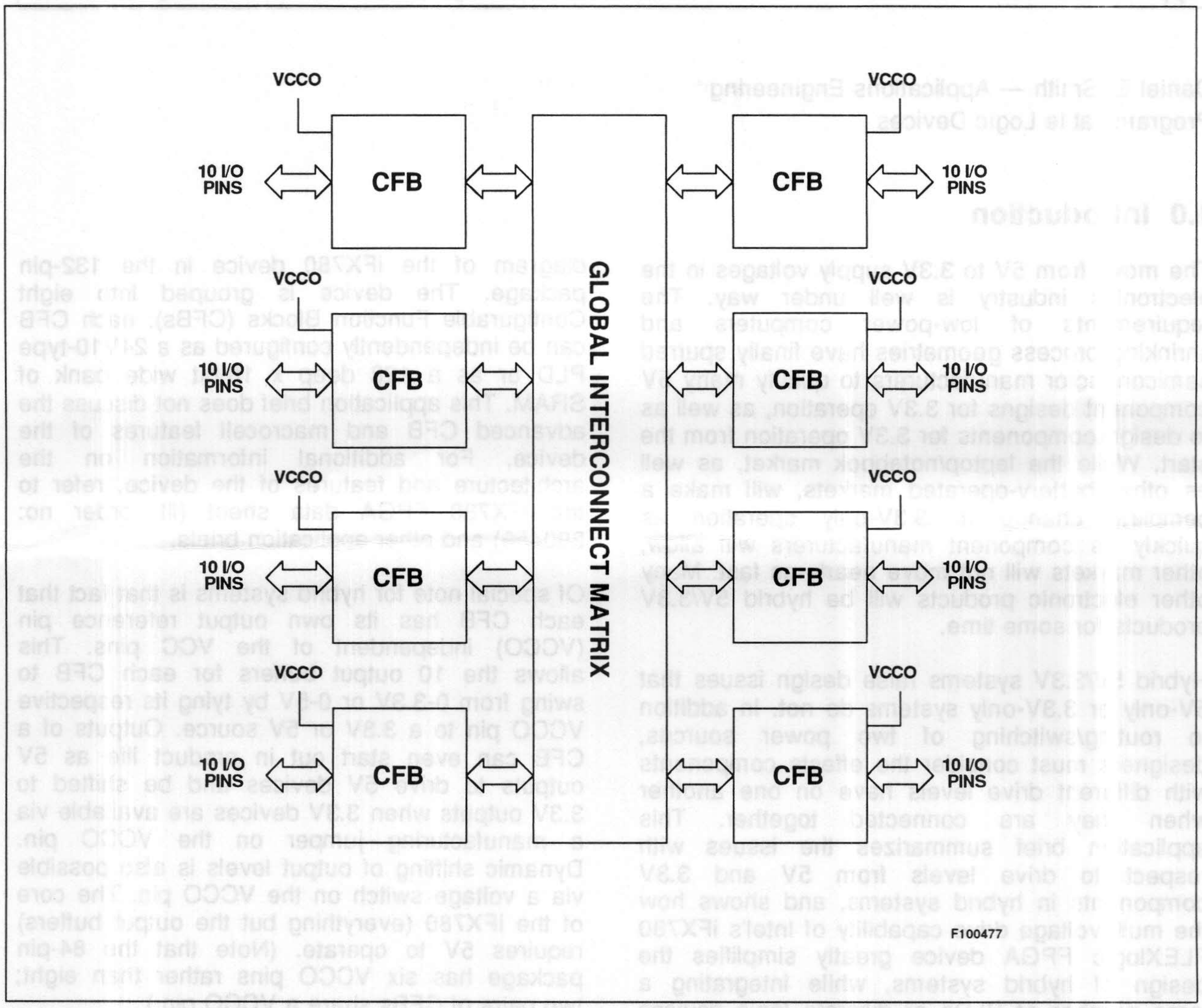
Figure 1. iFX780 Block Diagram Showing VCCO Pins



It also should be noted that inputs and I/O pin feedbacks on the iFX780 recognize 2.0V as a logic high. Input leakage vs. standby current can be matched to CMOS or TTL input levels. This is done on an input-by-input basis via another set of keywords, such as "TTL_LEVEL" or "CMOS_LEVEL". Inputs are configured during programming but can be changed via in-circuit reconfiguration.

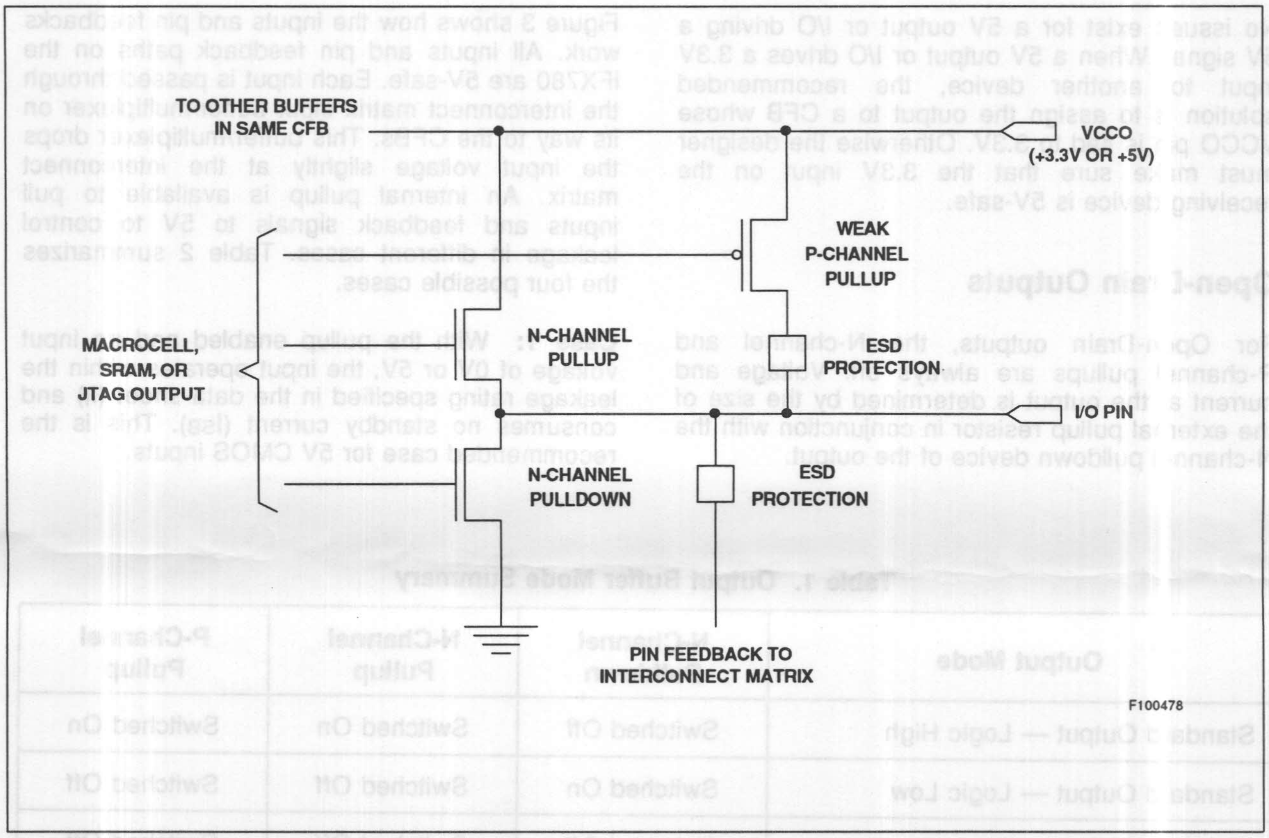
The following sections describe iFX780 output buffers and input buffers in more detail, and discuss power sequencing considerations for hybrid systems.

3.0 Output Buffer Considerations

Figure 2 shows how the output buffers work. Two N-channel devices on the left side of the diagram pull the output high or low, based on the inputs from the combinatorial or registered macrocell, SRAM, or the JTAG register. The pull-up device pulls outputs to approximately 3.0 volts. Both devices are switched off for high-impedance mode. For open-drain operation, the upper device is always off while the lower device is switched.

For logic high outputs, the weak P-channel device pulls the outputs past 3.0V to the level

Figure 2. iFX780 Output Buffer Equivalent Circuit



determined by the VCCO pin of a CFB. Thus any high level between 3.3V and 5V is supported by the output buffer. This P-channel device is switched off for high-impedance mode and is always off for open-drain operation. Table summarizes operation of the output buffers for different modes.

3.3V Outputs

No issues exist for a 3.3V output or I/O pin driving a 3.3V input or bus. When a 3.3V output or I/O is driving a 5V input, the high level of a 3.3V output is at least 2.4V, which exceeds the 2.0V minimum for a 5.0V input device. No translator is required; designers should, however, check to see if the receiving device leaks current at TTL levels (system power consideration).

When the 3.3V output or I/O is on a bus that includes both 3.3V and 5V devices, it is possible to drive a 5V high into the 3.3V output or I/O pin. The question naturally arises: "Will driving 5V into a 3.3V I/O pin latch up the output and therefore require that I use a translator/buffer?" For the iFX780, the answer is: "Definitely not." For shared bus applications, the N-channel pullup and the P-channel pullups are normally turned off when other devices are driving the bus (i.e., the iFX780 is in high impedance mode), otherwise bus contention would occur. Outputs, however, may be active for short periods of time during transitions and have 5V sourced even when in a high impedance state. Since all gate inputs to the N and P-channel devices are referenced to 5V, no leakage occurs. Design techniques have been employed that prevent the P-channel device from latching up. This same protection is present for I/O pins implementing inputs or bi-directional I/O. (The exception occurs during power-up and power-down; see "Power Sequencing" later in this brief.)

5V Outputs

No issues exist for a 5V output or I/O driving a 5V signal. When a 5V output or I/O drives a 3.3V input to another device, the recommended solution is to assign the output to a CFB whose VCCO pin is tied to 3.3V. Otherwise the designer must make sure that the 3.3V input on the receiving device is 5V-safe.

Open-Drain Outputs

For Open-Drain outputs, the N-channel and P-channel pullups are always off. Voltage and current at the output is determined by the size of the external pullup resistor in conjunction with the N-channel pulldown device of the output.

4.0 Input Buffer Considerations

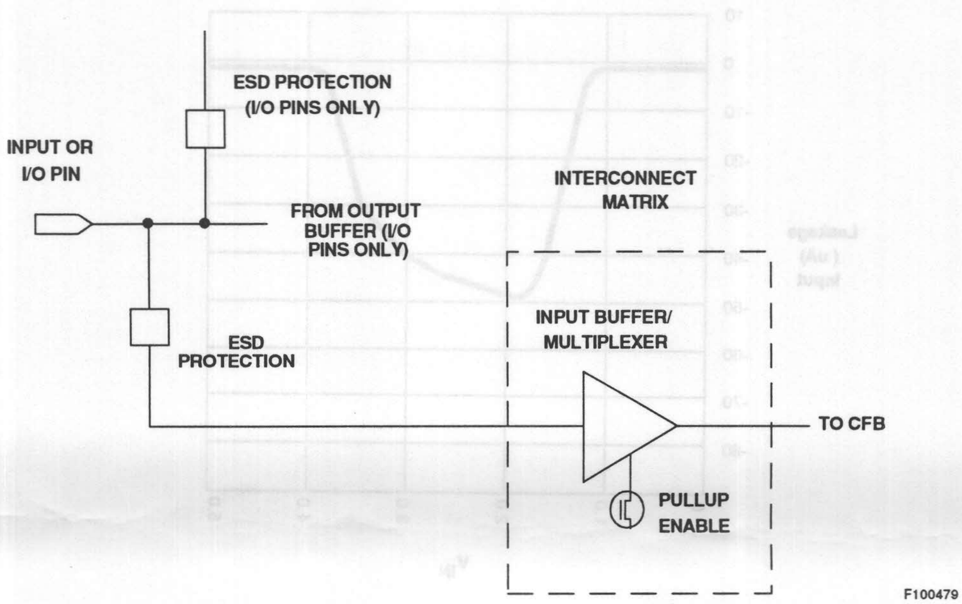
Figure 3 shows how the inputs and pin feedbacks work. All inputs and pin feedback paths on the iFX780 are 5V-safe. Each input is passed through the interconnect matrix input buffer/multiplexer on its way to the CFBs. This buffer/multiplexer drops the input voltage slightly at the interconnect matrix. An internal pullup is available to pull inputs and feedback signals to 5V to control leakage in different cases. Table 2 summarizes the four possible cases.

Case 1: With the pullup enabled and an input voltage of 0V or 5V, the input operates within the leakage rating specified in the data sheet (I_I) and consumes no standby current (I_{SB}). This is the recommended case for 5V CMOS inputs.

Table 1. Output Buffer Mode Summary

Output Mode	N-Channel Pulldown	N-Channel Pullup	P-Channel Pullup
Standard Output — Logic High	Switched Off	Switched On	Switched On
Standard Output — Logic Low	Switched On	Switched Off	Switched Off
Standard Output — High Impedance	Switched Off	Switched Off	Switched Off
Open-Drain Output — Logic High	Switched Off	Always Off (External Pullup)	Always Off (External Pullup)
Open-Drain Output — Logic Low	Switched On (Pulls Against External Pullup)	Always Off	Always Off
Open-Drain Output — High Impedance	N/A (External Pullup)	N/A(External Pullup)	N/A (External Pullup)

Figure 3. iFX780 Input Buffer Equivalent Circuit



Case 2: With the pullup enabled and an input voltage between 0V and 5V (e.g., being held at 3.0V by a TTL output), I_I will be higher than spec., causing I_{SB} to be higher. Figure 4 shows the leakage current at different voltage levels.

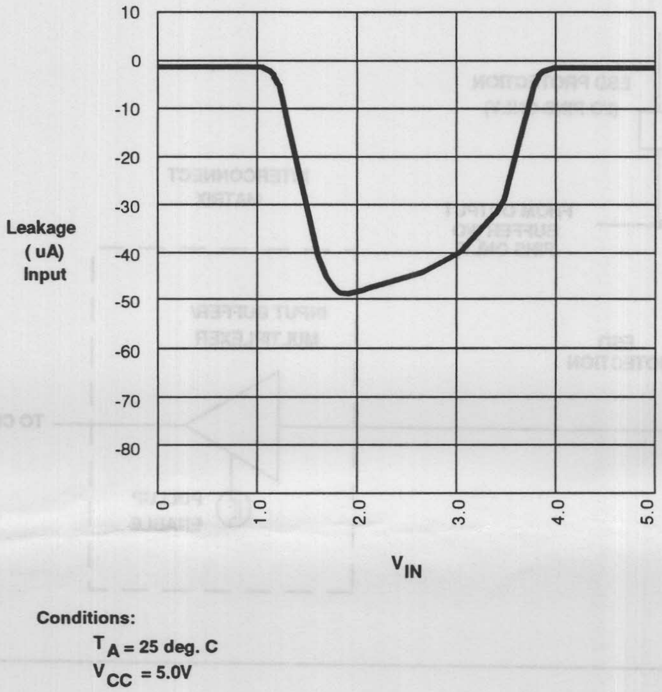
Case 3: With the pullup disabled and an input voltage of 5V, the internal voltage drop holds the input at approximately 3V. I_{SB} will be higher.

Case 4: For input signals between 0V and 3V, a designer can disable the pullup to bring the

Table 2. iFX780 Input Signal Level vs. Internal Pullup Options

Input Signal Level	Internal Pullup Enabled	Internal Pullup Disabled
V_{IH} = 5V	**Case 1:** $I_I \leq 10\ \mu A$ Low I_{SB} (Recommended for 5V CMOS)	**Case 3:** $I_I \leq 10\ \mu A$ Higher I_{SB}
V_{IH} = 3V	**Case 2:** I_I (See Figure 4) Higher I_{SB}	**Case 4:** $I_I \leq 10\ \mu A$ Higher I_{SB} (Recommended for TTL and 3V CMOS)

Figure 4. iFX780 Input Leakage Vs. Voltage — Pullup Enabled



leakage current back within spec. This is the recommended case for TTL or 3V CMOS inputs. It should be noted, however, that I_{SB} is 10-20% higher in this case than with case 2.

5.0 Power Sequencing

When all CFB outputs operate at 5V levels, no power sequencing is necessary for the iFX780. Power sequencing *is* required, however, when any or all CFBs operate at 3.3V levels. In this case, as is common with most devices and systems that use both 5V and 3.3V, the 5V source must be equal to or greater than the 3.3V source during power-up. During power-down, the 3.3V source must be less than or equal to the 5V source. This sequencing will prevent I/O latchup during power-up and reverse-bias through the VCC pins during power-down. Figure 5 shows this sequencing.

Figure 5. iFX780 5V/3.3V Power Supply Sequencing